India’s Semiconductor Ambitions: Building a Chip Ecosystem for 2030

A policy and industrial strategy paper on fabrication, design, packaging, materials, talent and governance

[1]Rachit Baijal
[1]Director General
[1]Artha-Niti Institute for Governance, India

***Abstract*—India's semiconductor strategy has moved from aspiration to execution. The country now seeks to transform a large electronics market and a deep engineering services base into a full-stack chip ecosystem by 2030. This paper examines the strategic logic, policy architecture, industrial constraints and institutional requirements of that ambition. It treats semiconductors not merely as a manufacturing vertical but as an enabling infrastructure for artificial intelligence, telecom, electric mobility, defence, healthcare, renewable energy, digital public infrastructure and high-value electronics exports. The study uses a policy-analytical method built around secondary data, official policy documents, public project announcements and comparative industrial strategy. It argues that India's strongest 2030 pathway is not a narrow attempt to duplicate Taiwan or South Korea, but a differentiated ecosystem model anchored in mature-node fabrication, compound semiconductors, advanced packaging, design-linked intellectual property, materials reliability, equipment servicing, talent pipelines and trusted global partnerships. The paper identifies five decisive bottlenecks: fabrication economics, technology transfer, supply-chain depth, process talent and inter-governmental coordination. It concludes with a sequenced roadmap for 2026 to 2030, recommending mission governance, demand aggregation, cluster discipline, fab-ready skilling, domestic procurement anchors, water and power planning, design-to-product incentives and a national semiconductor security framework.**

***Index Terms*—India Semiconductor Mission, chip ecosystem, semiconductor fabrication, OSAT, ATMP, fabless design, compound semiconductors, advanced packaging, electronics manufacturing, strategic autonomy, industrial policy.**

I. Introduction

Semiconductors have become the grammar of modern power. Every major technology platform that will define economic competitiveness in the coming decade depends on chips: artificial intelligence accelerators, mobile devices, electric vehicles, industrial robots, 5G and future 6G telecom equipment, defence electronics, satellites, medical devices, smart grids and secure digital public infrastructure. For India, therefore, the semiconductor question is not simply whether a fab can be built. It is whether the country can create a durable ecosystem in which design, fabrication, packaging, testing, materials, equipment maintenance, talent and market demand reinforce one another. India's 2030 ambition must be judged by that ecosystem standard rather than by headline investment alone.

The context has changed rapidly. The global chip industry is growing because AI infrastructure, data centres, automotive electrification and connected devices are raising semiconductor intensity across sectors. Deloitte expected the global semiconductor industry to approach US$975 billion in sales in 2026, while McKinsey argued that conventional estimates may understate the full value of the industry when in-house chip design and advanced packaging are considered [11], [12]. India sits at the intersection of this demand surge and global supply-chain realignment. It has a fast-growing domestic electronics market, strong software and design talent, geopolitical credibility as a trusted partner and a policy apparatus that has begun to shift from consumption-led import dependence to strategic production capability.

Yet semiconductor ecosystems are among the most difficult industrial systems to build. A fabrication plant is capital intensive, technologically unforgiving and operationally dependent on hundreds of upstream and downstream inputs. Yield discipline, contamination control, process integration, uninterrupted utilities, specialty chemicals, gases, ultrapure water, precision logistics and thousands of trained technicians are as important as headline capital. Unlike conventional manufacturing, a chip facility cannot be treated as an isolated factory. It requires a metropolitan-scale industrial operating system. The purpose of this paper is to examine what that operating system should look like for India by 2030.

The central argument is that India's semiconductor ambition should be ecosystem-led, sequenced and selective. India should pursue fabrication, but it should avoid measuring success only by the pursuit of the most advanced logic nodes. A more credible 2030 strategy is to dominate strategically useful domains: mature-node logic and analog chips, power semiconductors, sensors, microcontrollers, radio-frequency components, compound semiconductors, advanced packaging, automotive and industrial chips, secure chips for public infrastructure, and design intellectual property that can be embedded in Indian and global products. This pathway aligns better with India's domestic demand profile, existing talent base and current investment pipeline.

The paper uses the phrase chip ecosystem to describe the linked set of institutions, capabilities and markets that convert semiconductor demand into domestic value addition. This includes public policy, firm-level investment, technology partnerships, state industrial parks, skill systems, procurement anchors, environmental management, research institutions, financial instruments, export channels and regulatory trust. Building this ecosystem is a national development project, but it must be executed with industrial discipline. Ambition alone cannot produce yield; policy announcements alone cannot create process engineers; capital subsidy alone cannot create trusted supply chains. The transition from ambition to capability is the real research problem.

By 2030, India should aim to achieve four measurable outcomes. First, it should have multiple operational packaging and assembly facilities with export credibility. Second, it should have at least one stable mature-node fab ramping commercial output and connected to domestic demand. Third, it should have a larger pipeline of indigenous chip designs moving from prototype to product. Fourth, it should have created ecosystem depth in materials, sub-components, equipment servicing, utilities, design tools access and skilled technicians. The combination of these outcomes would mark the shift from symbolic entry into semiconductors to genuine ecosystem formation.

II. Research Problem, Objectives and Methodology

The research problem addressed in this paper is the gap between semiconductor aspiration and semiconductor ecosystem capability. India has announced and attracted major investments, but investment announcements do not automatically create strategic autonomy. Strategic autonomy requires the ability to design, package, manufacture, procure and maintain semiconductor supply for priority sectors under normal and stressed conditions. It also requires domestic value addition rather than mere location of facilities. The problem is therefore institutional and systemic: what should India build, how should the public sector coordinate it, and what capabilities must be prioritized before 2030?

The objectives are fourfold. First, the paper maps the structure of the semiconductor value chain and identifies where India has relative strengths and weaknesses. Second, it reviews the current Indian policy architecture, particularly the India Semiconductor Mission, the Design Linked Incentive scheme and the electronics manufacturing ecosystem. Third, it analyses bottlenecks in fabrication, packaging, talent, materials, infrastructure and governance. Fourth, it proposes a sequenced roadmap for building a credible chip ecosystem by 2030. The paper's orientation is policy-prescriptive rather than purely descriptive; it is designed to guide institutional action.

The methodology is qualitative and policy-analytical. It draws on official Government of India releases, public project announcements, industry forecasts, NITI Aayog material, global semiconductor analyses and comparative lessons from established semiconductor jurisdictions. The analysis is organized around an ecosystem maturity framework. Each capability is evaluated according to whether it is nascent, emerging, operational or globally competitive. This framework is useful because semiconductor capability cannot be reduced to binary categories such as having or not having a fab. A country may be strong in design execution but weak in manufacturing, strong in assembly but weak in substrate supply, or strong in policy incentives but weak in industrial operations.

The paper has three limitations. First, the semiconductor industry changes quickly, and project timelines, capacities and technology partnerships may evolve after public announcements. Second, some commercially sensitive details such as yield, customer mix, procurement terms and technology-transfer conditions are not publicly available. Third, projections for chip demand vary across sources. Accordingly, the paper treats numerical forecasts as directional rather than deterministic. The underlying strategic conclusion, however, remains robust: semiconductor demand will grow, supply chains will remain geopolitically sensitive, and India needs domestic capability across the value chain.

III. Why Semiconductors Matter for India in 2030

The semiconductor is a general-purpose strategic input. Its importance arises from the fact that it sits inside every modern system that processes, senses, stores or transmits information. In India's case, this has immediate implications for industrial policy, national security and social infrastructure. A shortage or external disruption in chips can affect mobile phones, medical devices, railway systems, defence platforms, energy grids, financial networks and public service delivery. The COVID-era chip shortage showed that semiconductor disruptions are not abstract risks; they can delay production, raise costs and expose the fragility of import-dependent supply chains.

India's digital public infrastructure also increases the strategic value of chips. Payments, identity, health platforms, public distribution systems, telecom networks and data centres require trusted hardware. As the country expands AI adoption in governance, agriculture, education, health and logistics, compute infrastructure will demand more specialized chips. The more digital the economy becomes, the more vulnerable it becomes to external control over semiconductors. Building domestic capability does not mean complete autarky, which is unrealistic in such a globally interdependent industry. It means reducing single-point dependency and ensuring trusted access in critical domains.

The demand-side case is strong. India's electronics manufacturing has expanded sharply over the last decade, and official data report growth in electronics goods production from roughly Rs.1.9 lakh crore in 2014-15 to roughly Rs.11.3 lakh crore in 2024-25 [10]. Mobile phone production and exports have also risen substantially, making India a major assembly and export base. This growth creates the platform for deeper value addition. Without semiconductor and component localization, India risks remaining a high-volume, low-value assembler. With chip ecosystem capability, it can convert electronics scale into technological depth.

The strategic case is equally important. Defence electronics, secure communications, satellite systems, drones, cyber infrastructure and critical public networks require assured access to chips. Mature-node chips are especially relevant because many defence, automotive and industrial systems prioritize reliability, longevity and qualification over leading-edge density. This gives India a practical entry point. A country does not need to start with the most advanced node to become strategically relevant. It needs dependable capability in the nodes and package types that power its real economy and security systems.

The developmental case concerns jobs, skills and regional industrialization. Semiconductor facilities create direct employment for technicians, process engineers, equipment specialists, quality-control staff and design professionals. More importantly, they generate indirect employment in chemicals, gases, logistics, construction, cleanroom services, maintenance, testing labs, electronics assembly and research services. If clusters are built well, they can upgrade regional economies and create high-skill manufacturing corridors. If built poorly, they can become isolated subsidy-driven assets. The difference lies in ecosystem planning.

By 2030, semiconductor capability should therefore be treated as a pillar of Viksit Bharat, not a prestige project. The national goal should be to embed semiconductor capability into India's broader industrial transformation: electric mobility, renewable energy systems, telecom equipment, defence production, medical technology, AI compute, smart agriculture and advanced manufacturing. When chips are integrated with domestic demand, technology partnerships and procurement anchors, the ecosystem becomes self-reinforcing.

IV. Understanding the Chip Ecosystem

A semiconductor ecosystem begins with product definition and ends with validated deployment in a system. The chain includes electronic design automation, intellectual property blocks, architecture design, verification, mask preparation, wafer fabrication, process chemicals, gases, silicon wafers, compound substrates, lithography and deposition tools, testing, dicing, assembly, packaging, reliability qualification, logistics, distribution and system integration. No single country controls the entire chain. Even leading semiconductor powers depend on partners. The realistic objective for India is therefore not total self-sufficiency in every input by 2030, but strategic depth in selected layers and trusted access in others.

Design is the upstream knowledge layer. India has long participated in global chip design as an engineering services hub, with many multinational design centres employing Indian engineers. The challenge is to move from service execution to product ownership. This requires domestic companies that own specifications, IP cores, reference designs and customer relationships. It also requires access to expensive EDA tools, prototyping routes and validation infrastructure. The Design Linked Incentive scheme addresses part of this gap by offering financial incentives and design infrastructure support across development and deployment stages [8].

Table 1. Semiconductor value chain and India's 2030 capability question

Layer	Core function	India 2030 question
Chip architecture and design	Specifications, IP cores, EDA tools, verification, firmware and product ownership.	Strong engineering base; ownership of domestic IP remains limited but improving through DLI.
Wafer fabrication	Cleanroom processing of wafers through lithography, deposition, etching, implantation and metrology.	Emerging; Dholera fab is a landmark mature-node project but ramp and yield are decisive.
ATMP and OSAT	Assembly, packaging, testing, marking and qualification of chips for system use.	Fastest near-term capability; multiple approved units can create scale and export credibility.
Compound semiconductors	GaN, SiC, sensors, RF and power devices for EVs, telecom, display and defence.	High-potential niche where India can build differentiated capability.
Materials, gases and chemicals	Silicon wafers, substrates, gases, chemicals, filters, cleanroom consumables and photoresist ecosystem.	Critical gap; requires long qualification cycles and upstream partnerships.
Equipment and services	Tool installation, maintenance, calibration, process control, spare parts and field engineering.	Underdeveloped; service depth is essential for uptime and yield.
Talent and research	Process engineers, technicians, design engineers, quality teams, materials scientists and researchers.	Large STEM base but limited fab-ready process talent; needs specialized training.

Fabrication is the most visible and capital-intensive layer. It involves transforming wafers into integrated circuits through hundreds of process steps. The economics are difficult because high utilization, yield learning and rapid technology cycles determine profitability. A fab must be matched to market demand and process capability. For India, mature nodes, analog, power management, display drivers, microcontrollers and specialized chips for automotive, industrial and telecom applications may offer a more credible early route than immediately competing at the leading edge.

Packaging and testing are increasingly strategic. As transistor scaling becomes more difficult and heterogeneous integration grows, advanced packaging can produce system-level performance gains even when individual chips are produced on different nodes. Outsourced Semiconductor Assembly and Test facilities and Assembly, Testing, Marking and Packaging units can therefore become national differentiators. NITI Aayog's recent semiconductor roadmap also emphasizes advanced packaging, compound semiconductors and design leadership as areas where India can leapfrog [14]. This aligns with India's current investment pipeline, which includes several packaging projects.

Materials and equipment are the hidden foundations. A fab requires high-purity gases, chemicals, photoresists, sputtering targets, silicon wafers, substrates, specialty valves, pumps, filters, cleanroom consumables and precision maintenance capabilities. Many of these inputs have long qualification cycles and concentrated global suppliers. If India focuses only on fabs while ignoring materials and equipment servicing, it will remain dependent and vulnerable. Ecosystem strategy must therefore include supplier development, standards labs, long-term offtake agreements and partnerships with firms from Japan, the United States, Europe, Taiwan, South Korea and friendly resource-rich countries.

Finally, the ecosystem requires governance. Semiconductor investments involve central ministries, state governments, investors, technology partners, universities, utilities, environmental regulators, customs authorities and downstream customers. Without a coordination mechanism, projects can face delays in land, water, power, permits, skill availability and supplier onboarding. A mission-mode structure should not only approve projects but also monitor readiness milestones, resolve bottlenecks, aggregate demand and ensure that industrial parks meet fab-grade standards.

V. India’s Policy Architecture

India's semiconductor policy has evolved from broad electronics promotion to targeted semiconductor ecosystem development. The India Semiconductor Mission was approved in December 2021 under the wider Semicon India Programme. Official material describes an incentive framework of Rs.76,000 crore, with fiscal support of up to 50 per cent for silicon fabs, compound semiconductor facilities, assembly and testing units and chip design [2]. The Mission's design is significant because it recognizes that fabrication, packaging, display, compound semiconductors and design require different incentive tools.

The public architecture has four principal components. The Scheme for Semiconductor Fabs offers fiscal support of up to 50 per cent of project cost on a pari-passu basis to approved applicants. A similar scheme exists for display fabs. The Compound Semiconductor and ATMP/OSAT scheme extends 50 per cent capital expenditure support to compound semiconductor, silicon photonics, sensors, discrete semiconductor and packaging units [1]. The Design Linked Incentive scheme provides financial incentives and access to design infrastructure for semiconductor designs, chipsets, systems-on-chip, IP cores and linked design activities [1], [8]. Together, these instruments form a capital-plus-knowledge support structure.

Budget 2026-27 announced the launch of India Semiconductor Mission 2.0 and proposed increasing the Electronics Components Manufacturing Scheme outlay to Rs.40,000 crore [3]. This is important because semiconductor strategy cannot be separated from electronics component strategy. Fabs and packaging units require downstream demand, while electronics manufacturers require domestic components to raise value addition. The ECMS expansion suggests that India is trying to connect chip policy with broader component localization, rather than treating semiconductors as a stand-alone prestige sector.

The investment pipeline has moved beyond policy intent. By December 2025, public information stated that ten semiconductor projects with total investment of about Rs.1.60 lakh crore had been approved across six states [2], [7]. In May 2026, two additional projects were approved under the India Semiconductor Mission, including a compound semiconductor and mini/micro-LED display facility and an OSAT facility in Gujarat [6]. The India Semiconductor Mission website also lists milestones related to Micron, Kaynes, HCL-Foxconn/India Chip, 3D glass packaging and other projects [1]. This indicates that the project base is widening across fabs, packaging, compound semiconductors and design.

However, policy architecture must now enter a second phase. The first phase was about attracting anchor investments. The second phase must be about execution discipline. Project approvals should be followed by construction, equipment installation, technology transfer, workforce preparation, supplier qualification, customer onboarding, reliability certification and export market access. India's 2030 success will depend less on how many projects are announced and more on how many facilities reach stable commercial output with competitive yields and meaningful domestic linkages.

A mature policy architecture should also incorporate sunset reviews and performance-linked disbursement. Capital support is justified because semiconductor fabs generate externalities and strategic benefits, but public support must be linked to milestones. These may include tool installation, line qualification, water recycling, local supplier development, training commitments, domestic customer contracts and export certifications. Without rigorous milestone governance, incentives can create capacity without capability.

VI. Project Pipeline and Emerging Clusters

The current project pipeline provides India with a practical opportunity to build clusters rather than scattered facilities. Gujarat has emerged as the most visible early hub, with Sanand and Dholera hosting ATMP, OSAT, fabrication and compound semiconductor projects. Assam has entered the semiconductor map through the Morigaon packaging project, while Uttar Pradesh, Odisha and other states are developing related projects, packaging facilities and semiconductor parks. This geographic spread can be beneficial if each cluster develops a clear specialization rather than replicating generic incentives.

The Dholera fab by Tata Electronics in partnership with PSMC is the most important fabrication marker. It was approved with an investment of Rs.91,000 crore, planned capacity of 50,000 wafer starts per month, and applications including 28 nm high-performance compute chips and power management chips for EV, telecom, defence, automotive and consumer electronics [4]. The significance lies not only in the capital size but in the learning that a fab ecosystem can generate: process discipline, utilities management, supplier qualification, tool servicing and local engineering.

Packaging investments offer a faster route to visible output. Tata Semiconductor Assembly and Test in Morigaon, Assam was announced with an investment of Rs.27,000 crore and capacity of 48 million chips per day, with indigenous advanced packaging technologies such as flip chip and integrated system-in-package [4]. CG Power, with Renesas and Stars Microelectronics, was announced in Sanand with Rs.7,600 crore investment and 15 million chips per day capacity for specialized chips [4]. Kaynes Semicon's Sanand unit was approved with Rs.3,300 crore investment and 60 lakh chips per day capacity [5]. These facilities can create packaging credibility if they secure customers, meet reliability standards and integrate with design and electronics firms.

The 2026 approvals also show movement toward differentiated niches. Crystal Matrix Limited is to establish an integrated compound semiconductor fabrication and ATMP facility in Dholera for mini/micro-LED display modules and GaN foundry services, while Suchi Semicon is to set up an OSAT facility in Surat for discrete semiconductors [6]. These projects matter because compound semiconductors and discrete devices are relevant to power electronics, displays, automotive systems, industrial automation and defence. India can create strategic relevance by focusing on these high-growth niches where domestic demand and global market gaps overlap.

Table 2. Selected public semiconductor projects relevant to India's 2030 ecosystem

Project	Location	Publicly stated scale or focus	Strategic relevance
Micron ATMP	Sanand, Gujarat	Memory assembly, testing, marking and packaging	Cabinet approval announced in 2023; ISM milestone notes production commencement in 2026.
Tata Electronics and PSMC fab	Dholera, Gujarat	Rs.91,000 crore; 50,000 WSPM; 28 nm and power management applications	Anchor mature-node fabrication project.
Tata Semiconductor Assembly and Test	Morigaon, Assam	Rs.27,000 crore; 48 million chips per day; flip chip and ISIP packaging	Major advanced packaging project in eastern India.
CG Power, Renesas and Stars Microelectronics	Sanand, Gujarat	Rs.7,600 crore; 15 million chips per day	Specialized chips for consumer, industrial, automotive and power applications.
Kaynes Semicon	Sanand, Gujarat	Rs.3,300 crore; 60 lakh chips per day	OSAT/packaging facility serving industrial, automotive, EV, telecom and consumer segments.
Crystal Matrix Limited	Dholera, Gujarat	Compound semiconductor fab and ATMP; mini/micro-LED and GaN services	Approved in 2026; niche in display and GaN value chain.
Suchi Semicon	Surat, Gujarat	OSAT facility; 1,033.20 million chips per annum	Discrete semiconductors for power electronics, analog ICs and industrial systems.

The cluster question is now central. A semiconductor cluster is not merely land plus subsidy. It needs anchor firms, supplier parks, training centres, metrology labs, logistics corridors, reliable utilities, customs facilitation, universities, housing, emergency services, waste management and industry governance. Sanand-Dholera can become a western semiconductor corridor if supplier networks and design houses are attracted around the anchor units. Morigaon can become an eastern packaging and electronics node if connectivity, talent housing, training and downstream assembly are strengthened. Uttar Pradesh and Odisha can develop specialized packaging and materials functions if they avoid fragmented industrial planning.

The risk is that states compete only through fiscal incentives. Semiconductor investors also require execution credibility, power quality, water reliability, cleanroom-ready construction ecosystems, quick approvals and skilled labour. A state offering more subsidy but weaker utilities may be less competitive than a state offering industrial certainty. The central government should therefore publish a semiconductor cluster readiness index covering water, power, land, logistics, skilling, academic linkages, environmental systems and project management. This would create healthy competition around capability rather than subsidy alone.

VII. Demand-Side Drivers and Market Formation

Semiconductor ecosystems mature when demand is visible. India has historically imported the majority of its chip requirements because domestic consumption was embedded within imported devices, kits and components. The rise of domestic electronics manufacturing changes this equation. As mobile phones, telecom products, automotive electronics, smart meters, solar inverters, medical devices, appliances and industrial systems are assembled or manufactured in India, the scope for domestic chip offtake increases. However, demand must be converted into bankable purchase commitments. Fabs and packaging units need credible customers, not merely macro forecasts.

India's chip demand is expected to grow strongly through 2030. PIB material has cited estimates that India's chip market could reach US$100-110 billion by 2030 [7], while Deloitte India projects approximately US$120 billion by 2030 and US$300 billion by 2035 [13]. The estimates differ, but their direction is consistent: domestic demand is rising rapidly. The highest-growth segments are likely to include mobile devices, wearables, automotive electronics, EV power systems, telecom networks, data centres, AI edge devices, consumer electronics and industrial automation.

Automotive and electric mobility are particularly important. Modern vehicles use microcontrollers, power management chips, sensors, display drivers, radar chips, battery-management systems and increasingly AI-capable processors. EVs raise demand for power semiconductors, especially silicon carbide and gallium nitride devices that improve efficiency and thermal performance. India has a large automotive market and a policy push for electrification. This creates a natural demand anchor for power electronics, analog chips, sensors and microcontrollers.

Telecom and digital infrastructure provide another demand anchor. India's 5G deployment and future 6G ambitions require radio-frequency components, baseband chips, optical communication devices, network processors and secure hardware modules. Domestic telecom equipment policy can align with semiconductor design and packaging. If Indian-designed telecom hardware uses Indian-designed chips and trusted packaging, the country can create an integrated technology stack. This is strategically important because telecom infrastructure is both an economic and security asset.

Energy transition will also raise chip demand. Solar inverters, grid management systems, smart meters, battery storage, electric charging infrastructure and industrial drives use power semiconductors and control chips. India's renewable energy targets and grid modernization agenda can therefore support domestic semiconductor demand. The government can use procurement standards, quality norms and domestic value-add incentives to create a predictable market for chips used in energy systems.

Public procurement can play a catalytic role, but it must be carefully designed. Defence, railways, energy utilities, telecom public sector entities and digital infrastructure agencies can aggregate demand for secure and reliable chips. This does not mean mandating domestic chips before they are reliable. Instead, procurement should create qualification pathways, pilot orders, long-term forecasts and reliability testing. A national demand registry for strategic chips could help investors identify where domestic offtake is possible and where technology partnerships are needed.

VIII. Design and Intellectual Property: From Services to Products

India's strongest existing semiconductor capability is design talent. Many global semiconductor companies operate design centres in India, and Indian engineers contribute to verification, physical design, embedded software, system architecture and validation. This talent base is an important asset, but it does not automatically translate into domestic semiconductor ownership. A design services economy earns engineering revenue; a product design ecosystem owns IP, captures margins and influences standards. The transition from services to products is one of India's most important 2030 challenges.

The Design Linked Incentive scheme is a response to this challenge. It supports semiconductor design across the full lifecycle, including integrated circuits, chipsets, systems-on-chip, systems and IP cores. It also offers access to design infrastructure through the ChipIN Centre, including EDA tools, IP repositories and multi-project wafer prototyping support [8]. The importance of this intervention lies in reducing entry barriers. Startups and MSMEs cannot easily afford industry-grade EDA tools or prototyping runs. Without shared infrastructure, the design ecosystem remains concentrated in large multinationals.

However, financial incentives alone cannot create product companies. Fabless success requires market insight, customer relationships, reference boards, firmware, packaging partners, certification, working capital and sales channels. Indian chip startups should be linked to domestic electronics manufacturers, defence labs, telecom equipment makers, automotive tier suppliers and public procurement pilots. A design that is never deployed in a product is a learning exercise; a design that enters a device becomes an industrial capability. The policy objective should therefore be design-to-product conversion.

India should define priority design missions. These could include secure microcontrollers for digital public infrastructure, power management ICs for EVs and inverters, analog front-end chips for medical devices, RF components for telecom, sensor interfaces for industrial automation, edge-AI accelerators for agriculture and surveillance systems, and trusted chips for defence applications. By focusing on use-case missions, India can avoid dispersing limited design incentives across too many unrelated projects. Mission-based design also allows government and industry to coordinate testing, packaging and procurement.

Universities must be integrated into the design ecosystem. The Chip2Startup and EDA infrastructure initiatives can expose students to practical design flows, but course design should go beyond theory. Students should learn verification, timing closure, design-for-test, packaging constraints, reliability, firmware and product integration. India needs chip architects, not only coders. Academic tape-outs, shared shuttle runs and national chip design challenges can build confidence, but they must be followed by commercialization support.

By 2030, India should target a portfolio of indigenous semiconductor IP blocks and product chips in selected domains. A realistic goal would be dozens of validated designs deployed in Indian products, with a few globally competitive fabless firms. This would be more valuable than a large number of prototypes without customers. The measure of design policy should be not only the number of supported startups but the number of qualified chips shipped, revenue generated and IP blocks reused across sectors.

IX. Fabrication Strategy: Mature Nodes, Reliability and Selective Leadership

Fabrication has symbolic value because it represents sovereign manufacturing capability. But fabs are not all the same. Leading-edge logic fabs require extreme capital, technology access, enormous scale and a customer base that can absorb rapid node transitions. Mature-node fabs, by contrast, serve analog, power management, display, automotive, industrial, microcontroller and mixed-signal markets where reliability and availability are often more important than transistor density. India's first major fab strategy should therefore prioritize mature-node excellence rather than leading-edge imitation.

The Dholera project provides a foundation for this approach. A 28 nm and power-management-oriented fab can serve important domestic and global markets if it achieves yield, reliability and cost discipline. Mature nodes are not obsolete; they are foundational for vehicles, telecom equipment, industrial electronics, appliances, defence systems and energy infrastructure. The world has repeatedly seen shortages in mature-node chips because capacity investment often chases leading-edge margins while the real economy depends on older nodes. India can exploit this structural gap.

A mature-node strategy should be linked to long lifecycle markets. Automotive and industrial customers require qualification, reliability and supply assurance over many years. Defence and infrastructure systems also value stable supply. India should create a national qualification platform that helps domestic fabs meet automotive, industrial, telecom and defence standards. Without qualification, local chips may fail to secure serious customers even if they are manufactured domestically. Reliability engineering must therefore be treated as a national capability.

Fabrication also requires process learning. Yield does not appear automatically after equipment installation. It improves through disciplined measurement, defect reduction, recipe optimization, maintenance, contamination control and experienced engineering. India should invite global process experts, create returnee talent pathways and allow flexible hiring of foreign specialists where domestic capacity is insufficient. A fab without experienced process leadership is a high-risk asset. Talent policy must be aligned with technology-transfer policy.

The country should also avoid over-fragmentation. Too many small fabs without customer depth could weaken the ecosystem. A limited number of carefully supported fabs, each matched to a technology niche and demand base, is preferable. Possible niches include 28 nm logic and mixed signal, analog and power management, display drivers, MEMS sensors, silicon photonics, silicon carbide, gallium nitride and secure chips. Each fab should have an explicit customer strategy before public incentives are committed.

By 2030, the key metric is not whether India announces a leading-edge node. The metric is whether India can operate a fab with stable yield, credible customers, domestic supplier linkages, export capability and trained process teams. Once that base exists, the country can climb the technology ladder. Without it, advanced-node aspirations will remain dependent on external partners and vulnerable to financial stress. Fabrication strategy must therefore proceed from reliability to complexity.

X. Packaging, Testing and the More-than-Moore Opportunity

Packaging is no longer a low-value back-end process. As chiplets, heterogeneous integration, system-in-package, high-bandwidth memory, fan-out packaging and 2.5D/3D integration expand, packaging increasingly determines performance, power efficiency and system cost. This is why advanced packaging has become strategically important. India can enter this layer faster than it can enter leading-edge fabrication, and it can build export relevance if facilities meet global quality and reliability standards.

India's approved pipeline is heavily weighted toward ATMP and OSAT facilities. This is not a weakness; it may be the most pragmatic near-term route. Packaging units can support global and domestic chip companies, create technician employment, deepen reliability testing, and connect to electronics manufacturing. They can also provide a bridge for Indian design startups that need packaging and validation support. If design, packaging and electronics assembly are co-located or closely linked, India can create a cycle of product iteration.

Advanced packaging is especially relevant for AI, telecom, automotive and defence. These sectors often require system-level integration rather than a single monolithic chip. For example, an automotive electronics module may combine sensors, power devices, microcontrollers and communication chips. A telecom module may combine RF, baseband and power components. Defence systems may require ruggedized packaging and secure supply. India can develop specialized packaging capabilities aligned with these markets.

The policy challenge is to avoid becoming only a low-cost packaging location. Basic assembly has lower margins and can be vulnerable to competition. India's goal should be capability upgrading: flip chip, system-in-package, wafer-level packaging, reliability labs, thermal management, substrate development, failure analysis and design-for-package expertise. This requires R&D partnerships, standards labs, university programs and customer-driven qualification. A packaging plant should be surrounded by a testing and reliability ecosystem.

Substrates are a major bottleneck. Advanced packaging depends on high-quality substrates, interposers and materials. Global shortages and concentration in a few countries have exposed the fragility of this layer. India should identify packaging substrates, lead frames, bonding wires, thermal interface materials and cleanroom consumables as priority components under ECMS and related schemes. Without these inputs, packaging units may remain import-dependent even when final assembly occurs in India.

The phrase More-than-Moore captures the opportunity. Instead of competing only by shrinking transistor nodes, countries can create value through integration, packaging, power efficiency, sensors and system architecture. NITI Aayog's roadmap emphasizes that India should become an ecosystem player in this era, focusing on advanced packaging, system integration and manufacturing scale [14]. This is arguably India's most credible path to global relevance by 2030.

XI. Compound Semiconductors and Strategic Niches

Compound semiconductors such as gallium nitride and silicon carbide are important because they perform functions that conventional silicon cannot perform as efficiently in high-power, high-frequency or high-temperature environments. They are critical for EV power electronics, fast chargers, renewable energy systems, radar, RF communication, satellite systems, defence electronics and advanced displays. India's industrial and strategic demand profile makes compound semiconductors a natural priority.

The approval of a compound semiconductor and mini/micro-LED display facility in Dholera indicates policy movement in this direction [6]. Such projects can connect display technology, GaN foundry services and advanced packaging. India should not treat compound semiconductors as a peripheral segment. They are central to electric mobility, energy transition, telecom and defence. A focused GaN and SiC strategy can give India a niche that is technologically advanced but not as inaccessible as leading-edge silicon logic.

Silicon carbide is particularly relevant to EVs and power systems. It enables higher efficiency, faster switching and better thermal performance in inverters, chargers and industrial drives. Gallium nitride is important for fast chargers, RF systems, radar and mini/micro-LED display technologies. India should map domestic demand from EV manufacturers, renewable energy firms, telecom equipment makers and defence organizations, then use that demand to support domestic compound semiconductor manufacturing and packaging.

The ecosystem for compound semiconductors requires upstream materials and device-level expertise. Wafers, epitaxy, device design, packaging and reliability testing are all critical. India should create centres of excellence focused on power devices, RF devices and display technologies. These centres should be linked to industry projects, not isolated academic labs. A national compound semiconductor consortium could coordinate research, prototyping, qualification and procurement.

Strategic niches also include sensors, MEMS, silicon photonics, secure elements and radiation-hardened or ruggedized chips for space and defence. India has domestic demand and public institutions that can support these niches. The point is not to cover every niche immediately, but to select those where India has demand, talent and security needs. By 2030, niche leadership in a few high-value segments may be more valuable than shallow participation across many.

XII. Materials, Equipment and Supply-Chain Depth

The weakest link in many emerging semiconductor strategies is the upstream supply chain. A chip facility depends on inputs that must meet extraordinary purity and consistency requirements. Specialty gases, process chemicals, silicon wafers, substrates, photomasks, photoresists, filters, cleanroom garments, ultrapure water systems, pumps, valves and metrology tools all need reliable supply. A shortage or quality failure in one input can disrupt production. This is why semiconductor security cannot be achieved by building a fab alone.

India should classify semiconductor materials and equipment services into three categories. The first category includes inputs that can be localized relatively quickly, such as cleanroom consumables, certain chemicals, packaging materials, lead frames and maintenance services. The second includes inputs that require technology partnerships, such as substrates, specialty gases, high-purity chemicals and metrology support. The third includes inputs that will remain externally sourced for the near future, such as advanced lithography equipment and certain photoresists. A realistic strategy should deepen categories one and two while securing trusted access to category three.

The Electronics Components Manufacturing Scheme can support this supplier depth if its implementation is aligned with semiconductor requirements. Component localization should not be limited to smartphone assemblies. It should include semiconductor-adjacent materials, substrates, connectors, high-density printed circuit boards, camera modules, precision enclosures, thermal materials and power electronics components. The boundary between electronics components and semiconductor ecosystems is increasingly porous. A chip ecosystem requires both.

Equipment servicing is another high-leverage area. India may not manufacture advanced lithography tools by 2030, but it can develop installation, calibration, maintenance and field engineering capabilities for semiconductor equipment. Tool uptime is central to fab economics. If every maintenance problem requires external intervention, ramp-up becomes slow and costly. Equipment suppliers should be incentivized to create Indian service academies, spare-parts depots and field engineering teams.

Critical minerals and upstream resource partnerships also matter. Semiconductor and electronics supply chains require minerals, rare gases and refined materials that can become geopolitical chokepoints. NITI Aayog's roadmap identifies critical minerals and upstream partnerships as part of a long-term semiconductor strategy [14]. India should align its critical minerals policy, overseas resource partnerships and semiconductor mission. This includes long-term offtake agreements, recycling, strategic reserves and friendly-country processing partnerships.

Supply-chain depth should be measured. India should publish annual semiconductor value-chain localization indicators: percentage of domestic packaging materials, gases, chemicals, substrates, equipment services, design IP, testing capacity and qualified suppliers. This would move the debate beyond binary claims of self-reliance. The goal is not to pretend that everything is domestic; it is to know exactly where dependence remains and reduce critical vulnerabilities.

XIII. Talent, Skills and Research Capacity

Semiconductor production is a talent-intensive activity. It requires different categories of human capital: chip architects, verification engineers, process integration engineers, equipment technicians, cleanroom operators, materials scientists, reliability engineers, quality-control specialists, firmware developers and industrial project managers. India's engineering base is large, but fab-ready talent is limited because the country has not historically operated large commercial fabs. This creates a mismatch between general technical education and semiconductor operational needs.

A national semiconductor talent pyramid should be built. At the top are PhD-level researchers in materials, devices, architectures and process technology. In the middle are engineers trained in design, verification, process control, packaging, reliability and product engineering. At the base are technicians trained in cleanroom protocols, tool operation, safety, maintenance, quality systems and shift-based manufacturing discipline. A fab cannot run only on elite engineers; it needs thousands of disciplined technicians. India's skilling system must recognize this.

Universities should be assigned differentiated roles. IITs and leading research institutions can focus on device research, advanced packaging, compound semiconductors, design architecture and prototyping. State technical universities can develop process and manufacturing programs. Polytechnics and ITIs near semiconductor clusters should train technicians in cleanroom operations, equipment maintenance, industrial safety and quality control. Cluster-specific skilling is crucial because semiconductor facilities require workers who can live near the plant, work shifts and follow strict protocols.

Industry-led curriculum is necessary. Semiconductor courses designed without firms often remain theoretical. Companies should co-design modules, provide equipment exposure, sponsor labs, offer apprenticeships and define job roles. The government can support this by funding semiconductor finishing schools near major clusters. These schools should not only teach electronics theory; they should train students in statistical process control, failure analysis, yield basics, contamination control, electrostatic discharge, cleanroom behavior, preventive maintenance and industrial documentation.

India also needs global talent infusion. Experienced process engineers, packaging specialists and equipment experts from Taiwan, Japan, South Korea, Singapore, the United States and Europe can accelerate learning. Immigration and professional mobility rules should allow semiconductor projects to hire global experts quickly. At the same time, Indian diaspora professionals should be encouraged to return through tax, research and leadership incentives. Talent transfer is as important as technology transfer.

Research capacity should be linked to manufacturing problems. Too often, academic research and industrial production operate in parallel. India should create mission-oriented research calls in areas such as GaN devices, SiC packaging, thermal management, photonics, secure hardware, low-power AI chips, reliability testing, substrates and process chemicals. Grants should require industry participation and deployment pathways. By 2030, the research system should not only publish papers; it should solve bottlenecks faced by Indian semiconductor firms.

XIV. Infrastructure, Environment and Industrial Discipline

Semiconductor infrastructure is unforgiving. Fabs require uninterrupted high-quality power, ultrapure water, advanced waste treatment, vibration control, cleanroom-grade construction, reliable logistics and emergency response systems. Packaging units require less water than fabs but still need cleanrooms, power stability, testing labs and logistics. If infrastructure is weak, capital subsidy cannot compensate. India must therefore treat semiconductor parks as national infrastructure projects, not ordinary industrial estates.

Power quality is as important as power availability. Semiconductor tools can be sensitive to voltage fluctuations, outages and harmonics. A fab-grade power system requires redundancy, backup, monitoring and rapid restoration. States competing for semiconductor projects should provide dedicated substations, grid reliability commitments and green power options. Energy costs also matter because semiconductor manufacturing is electricity-intensive. Long-term power contracts can reduce uncertainty for investors.

Water is a major planning issue. Wafer fabrication requires large quantities of water and sophisticated recycling. In water-stressed regions, semiconductor projects can generate public concern unless recycling, treatment and allocation are transparently managed. India should require every fab project to publish water stewardship plans, including recycling targets, treatment methods and community safeguards. This is not merely environmental compliance; it is social license to operate. Semiconductor development cannot be sustainable if local communities perceive it as competing with drinking water or agriculture.

Environmental regulation should be rigorous but predictable. Semiconductor processes use chemicals and gases that require strict handling. Regulators must develop specialized capacity to evaluate semiconductor environmental management. Delayed approvals can hurt projects, but weak regulation can create long-term risks. A better approach is specialized fast-track regulation with high standards, technical expertise and continuous monitoring. Environmental credibility will also matter for export customers who evaluate supply-chain sustainability.

Logistics and customs facilitation are also important. Semiconductor equipment is expensive, delicate and time-sensitive. Delays in customs clearance, port handling or transportation can disrupt project timelines. India should create semiconductor green channels for approved projects, including pre-clearance of equipment, specialized transport protocols and rapid customs resolution. This does not mean weaker scrutiny; it means predictable and expert handling of specialized imports.

Industrial discipline is cultural as well as infrastructural. Semiconductor manufacturing requires precision, documentation, cleanliness, punctuality, preventive maintenance and process adherence. India's manufacturing systems have improved, but semiconductor-grade discipline must be deliberately cultivated. Every cluster should have quality culture programs, supplier certification, Six Sigma training and reliability audits. The ecosystem should reward operational excellence, not merely investment size.

XV. Finance, Incentives and Risk Sharing

Semiconductor projects require large capital commitments and long payback periods. Private investors face demand risk, technology risk, execution risk, policy risk and geopolitical risk. Public incentives are therefore common across semiconductor jurisdictions. The United States, European Union, Japan, South Korea, Taiwan and China have all used public support to attract or retain semiconductor investment. India is not unusual in using incentives; the real question is whether incentives are structured to create durable capability.

Capital subsidies reduce entry barriers, but they must be complemented by patient finance. Fabs require debt structures that understand long construction periods, foreign currency equipment costs and ramp-up uncertainty. Indian financial institutions may need specialized semiconductor appraisal capacity. A national semiconductor finance facility could combine public support, development finance, sovereign guarantees, export credit and private capital. Such a facility should be professionally managed and linked to technical due diligence.

Risk sharing should be conditional. Public funds should support projects that bring technology access, customer commitments, local supplier development, training and export potential. Incentives should be disbursed against milestones rather than promises. These milestones may include land readiness, financial closure, technology agreements, equipment orders, cleanroom completion, line qualification, production start, yield targets and customer certification. This protects public money and improves execution discipline.

Demand-side incentives can be as important as supply-side incentives. If domestic electronics firms are encouraged to use qualified Indian chips, packaging or components, investors gain offtake confidence. This can be done through procurement preference, tax benefits, standards, pilot programs and viability support. However, domestic preference must not compromise quality. The correct sequencing is qualification first, preference second. A low-quality domestic chip can damage confidence in the ecosystem.

India should also consider anchor customer contracts for strategic chips. Defence, railways, energy utilities, telecom networks and public digital infrastructure agencies can provide long-term demand signals for secure microcontrollers, power devices, sensors and communication chips. Such contracts should include reliability standards, price bands and upgrade pathways. They can help domestic firms plan capacity while giving public agencies trusted supply.

Finally, incentives should support exit and restructuring where needed. Semiconductor projects can fail or change direction. A rigid subsidy system may keep weak projects alive, while a mature system allows consolidation, technology pivoting or asset transfer. The goal is ecosystem capability, not preservation of every approved project. Policy should be flexible enough to reallocate support from underperforming projects to stronger ones, while maintaining transparency and accountability.

XVI. Global Lessons for India

Taiwan's semiconductor success rests on focused industrial strategy, technical depth, supplier ecosystems and deep integration with global customers. It did not emerge overnight. It required institutions, state support, technology acquisition, diaspora talent, customer trust and relentless operational discipline. The lesson for India is not that Taiwan can be copied. Taiwan's scale in leading-edge foundry services emerged from specific historical and geopolitical conditions. The transferable lesson is ecosystem coherence: design houses, foundries, suppliers, universities and government agencies evolved together.

South Korea demonstrates the power of large conglomerates, memory leadership and export-oriented manufacturing. Samsung and SK Hynix combine scale, capital, R&D and manufacturing experience. India does not yet have equivalent semiconductor manufacturing champions, but large Indian groups are now entering the sector. The lesson is that national champions can matter, but they must be technologically capable and globally competitive. Protection without performance will not create semiconductor leadership.

The United States shows the enduring importance of design, EDA tools, equipment, research universities and venture capital. Even where fabrication migrated abroad, the United States retained dominance in chip architecture, design software, equipment and high-value innovation. India should learn from this by strengthening design IP, EDA access, research and startup ecosystems. A country can be strategically powerful in semiconductors without controlling every fab, if it owns critical knowledge layers.

Japan's strength lies in materials, chemicals, equipment and manufacturing quality. Many global semiconductor supply chains depend on Japanese materials and tools. This is a crucial lesson for India because upstream supply chains receive less public attention than fabs. India should pursue partnerships with Japanese firms in gases, chemicals, wafers, equipment servicing, quality systems and materials research. Supplier depth can become a source of strategic leverage.

China shows the scale and limits of state-led ambition. Massive investment can expand capacity and create firms, but export controls, technology chokepoints and dependence on advanced tools can constrain progress. The lesson for India is that semiconductor policy must be geopolitically aware. Trusted partnerships matter. India should avoid isolation, build with partners and ensure that its ecosystem is acceptable to global supply chains. Strategic autonomy in semiconductors is achieved through trusted interdependence, not isolation.

The European Union offers another lesson: semiconductor strategy must connect to industrial demand. Automotive, industrial automation, energy and telecom sectors shape Europe's chip priorities. India's strategy should similarly be demand-led. Instead of seeking prestige nodes disconnected from domestic markets, India should align chip capability with EVs, telecom, renewable energy, defence, medical devices and digital infrastructure. The most resilient semiconductor ecosystems are those tied to real industrial demand.

XVII. Risks and Bottlenecks

The first risk is execution delay. Semiconductor projects have complex construction and equipment timelines. Delays can arise from land, utilities, permits, cleanroom readiness, imported equipment, workforce shortages or financing. In a fast-moving industry, delays can affect technology relevance and customer confidence. India needs project management units with technical capacity to monitor each approved project. Traditional bureaucratic review is insufficient for semiconductor execution.

The second risk is technology-transfer shallowness. A facility may be located in India but remain dependent on foreign technology partners for recipes, process know-how, customer relationships and maintenance. Partnerships are necessary, but they should include capability development. Contracts should specify training, localization, Indian leadership pipelines, supplier development and knowledge transfer where commercially feasible. Without this, India may host assets without owning capability.

The third risk is insufficient domestic value addition. Packaging or assembly facilities may import almost all inputs and perform limited operations. This still creates some jobs and strategic value, but the broader ecosystem remains thin. India should track value addition and supplier development over time. A facility should be expected to deepen local linkages gradually, not instantly. A transparent localization roadmap can prevent both unrealistic expectations and complacency.

Table 3. Principal bottlenecks and policy responses

Bottleneck	Why it matters	Policy response
Execution delay	Land, utilities, equipment imports, permits and cleanroom readiness can slow projects.	Technical project management units, milestone dashboards and rapid inter-agency resolution.

Bottleneck	Why it matters	Policy response
Technology-transfer gaps	Facilities may depend heavily on foreign partners without deep local learning.	Training clauses, Indian leadership pipelines, joint R&D and supplier localization targets.
Thin supplier base	Materials, gases, substrates and equipment services may remain import-dependent.	Supplier parks, ECMS alignment, standards labs and trusted country partnerships.
Talent shortage	Fab-ready process and technician talent remains limited.	Cluster finishing schools, apprenticeships, diaspora return pathways and global expert hiring.
Environmental stress	Water, chemicals and waste can create social risk.	Water recycling mandates, transparent environmental audits and community benefit plans.
Demand uncertainty	Macro demand may not convert into bankable offtake.	Demand registry, anchor procurement and qualification pathways for strategic sectors.

The fourth risk is talent scarcity. Process engineers, equipment technicians and reliability specialists cannot be created overnight. If multiple facilities ramp simultaneously, they may compete for the same limited workforce. This can raise costs and slow operations. Talent planning must precede production. Semiconductor skilling should begin before factories open, with apprenticeships, overseas training and cluster-based finishing schools.

The fifth risk is environmental and social resistance. Water use, chemical handling and land acquisition can generate local concerns. If communities see semiconductor projects as elite enclaves with limited local benefits and high resource use, opposition may rise. Transparent environmental management, local hiring, supplier development and community engagement should be part of cluster governance from the beginning. Social legitimacy is a strategic asset.

The sixth risk is global market cyclicality. Semiconductor markets are cyclical, with periods of shortage and oversupply. Public policy must avoid assuming permanent scarcity. Investments should be evaluated against long-term demand, not temporary price spikes. India can reduce cyclical vulnerability by focusing on strategic domestic demand, diversified applications and long-lifecycle markets such as automotive, industrial, energy and defence.

XVIII. 2030 Roadmap: Sequencing the Ecosystem

A credible roadmap must sequence capability. India cannot build every layer simultaneously at world scale, but it can create cumulative momentum. The period from 2026 to 2030 should be divided into four phases: execution stabilization, supplier deepening, demand anchoring and global integration. Each phase should have measurable milestones. Announcements should give way to dashboards. The ecosystem should be judged by operational output, domestic value addition, talent creation and export credibility.

In 2026-27, the priority should be project execution and institutional strengthening. Approved facilities should receive intensive coordination support. Cluster utilities, customs processes, skilling programs and supplier identification should be completed before equipment ramp. ISM 2.0 should define a detailed implementation architecture, including separate verticals for fabs, packaging, design, materials, talent and demand. Every major project should have a public readiness status that avoids disclosing sensitive data but indicates progress.

Table 4. Sequenced roadmap for chip ecosystem formation

Period	Strategic focus	Core milestones
2026-27	Execution stabilization	Operationalize ISM 2.0, accelerate approved projects, complete cluster utilities, begin fab-ready skilling and supplier mapping.
2027-28	Ramp and qualification	Packaging output, reliability labs, design-to-product pilots, anchor procurement in defence, telecom, EV and energy sectors.
2028-29	Supplier deepening	Localize priority gases, chemicals, substrates, cleanroom consumables and equipment services; strengthen cluster specialization.
2029-30	Global integration	Export-qualified OSAT and ATMP, mature-node fab output, domestic chip products in market and trusted partnerships.
Beyond 2030	Capability upgrading	Advanced packaging scale, compound semiconductor leadership, selective node upgrades and deeper equipment/materials ecosystem.

In 2027-28, the priority should be production ramp and design-to-product conversion. Packaging units should secure domestic and export customers. Indian design startups should be matched with packaging and electronics firms. Strategic sectors should begin pilot procurement of qualified domestic chips and packages. Reliability labs should certify products for automotive, industrial, energy, telecom and defence applications. Universities near clusters should produce the first large cohorts of fab-ready technicians.

In 2028-29, the priority should be ecosystem deepening. Supplier parks should localize selected materials, chemicals, cleanroom consumables, substrates and equipment services. State clusters should specialize: one cluster may focus on fabrication and analog chips, another on advanced packaging, another on compound semiconductors, another on design and prototyping. A national semiconductor value-chain index should track progress. Public incentives should shift gradually from capital attraction to performance, yield, exports, localization and R&D.

By 2029-30, the priority should be global credibility. Indian facilities should be integrated into trusted global supply chains. Domestic fabless firms should have products in market. Packaging facilities should meet global customer audits. Mature-node fabrication should demonstrate reliability and customer qualification. India should host semiconductor standards forums, export promotion missions and technology partnerships. The objective should be to make India not merely a market for chips but a reliable node in global semiconductor production.

The roadmap must remain adaptive. Semiconductor technology and geopolitics will change. AI demand could accelerate advanced packaging; EV growth could raise SiC demand; export controls could alter equipment access; global oversupply could pressure prices. India should review the roadmap annually and adjust incentives, technology priorities and partnerships. A successful semiconductor mission is not a static plan but a learning institution.

XIX. Policy Recommendations

First, India should establish a Semiconductor Ecosystem Council chaired at the highest appropriate level and supported by a professional technical secretariat. The council should include MeitY, ISM, finance, commerce, heavy industries, defence, railways, power, NITI Aayog, state governments, industry and academia. Its mandate should be bottleneck resolution, demand aggregation, supplier development, skill alignment and progress monitoring. Semiconductor policy cannot be fragmented across ministries.

Second, India should create a national semiconductor demand registry. Strategic sectors should identify the chips they need over five to ten years, including specifications, volumes, qualification standards and security requirements. This registry would help domestic designers, fabs and packaging units understand where demand exists. It would also help policymakers identify which chips are critical for resilience and which can be sourced through normal global markets.

Third, incentives should be linked to ecosystem obligations. Large projects receiving public support should commit to training, supplier development, environmental standards, local procurement targets where feasible, R&D collaboration and periodic reporting. The objective is not to burden investors but to ensure that public support creates public capability. The strongest semiconductor jurisdictions use incentives to shape ecosystems, not simply to attract factories.

Fourth, India should build national reliability and qualification labs. These labs should support automotive, industrial, telecom, defence, medical and energy chip qualification. They should offer failure analysis, thermal testing, vibration testing, electrostatic discharge testing, life-cycle testing and packaging validation. Without such labs, Indian chips will struggle to gain customer trust. Qualification infrastructure is as important as fabrication infrastructure.

Fifth, India should create semiconductor supplier parks linked to anchor facilities. These parks should target materials, gases, chemicals, substrates, cleanroom consumables, equipment services, packaging inputs and precision logistics. Supplier parks should be planned with long-term offtake agreements and quality standards. Localization should begin with feasible inputs and gradually move toward more complex ones. This is how supply-chain depth is built.

Table 5. Policy priorities for a 2030 semiconductor ecosystem

Priority area	Recommended action
Mission governance	Create a technical semiconductor ecosystem council with authority to resolve bottlenecks.
Demand anchoring	Build a strategic chip demand registry for defence, telecom, EV, energy, health and digital infrastructure.
Supplier depth	Use ECMS and cluster policy to localize gases, chemicals, substrates, packaging inputs and equipment services.
Talent	Launch fab-ready technician and process engineer programs around clusters.
Design commercialization	Move DLI from prototype support to product deployment and customer acquisition.
Reliability infrastructure	Create national labs for qualification, failure analysis and standards testing.
Environmental trust	Mandate water recycling, chemical safety and transparent community safeguards.
Global partnerships	Structure trusted-country collaborations around technology transfer, talent and market access.

Sixth, the country should launch a Fab-Ready India skilling mission. The mission should train technicians, process engineers and equipment specialists through cluster-based finishing schools, apprenticeships and international partnerships. It should include certification standards and job-role definitions. Talent should be treated as a production input, not as a general education outcome. Every major project should have a talent pipeline plan.

Seventh, India should deepen design-to-product support. The DLI scheme should be connected to domestic procurement pilots, packaging partners, MPW prototyping, reference boards, standards testing and commercialization finance. Startups should be rewarded not only for tape-outs but for chips deployed in products. A design productization fund could support the expensive transition from prototype to validated market-ready chip.

Eighth, water and environmental governance should be standardized. Every semiconductor cluster should have water recycling targets, chemical handling protocols, waste treatment systems and community transparency mechanisms. India can build a sustainable semiconductor ecosystem if environmental discipline is integrated from the beginning. Sustainability should become a competitive advantage, especially for global customers with supply-chain ESG requirements.

Ninth, India should pursue trusted international partnerships. The country should work with the United States, Japan, Taiwan, South Korea, Singapore, the European Union and resource-rich partners. Partnerships should be structured for technology access, training, supplier linkages, equipment servicing, research collaboration and market access. Semiconductor autonomy is not isolation; it is the ability to participate in global networks from a position of capability.

Tenth, India should publish an annual Semiconductor Ecosystem Report. The report should track projects, output, value addition, talent, research, supplier localization, exports, water performance, design deployments and strategic chip availability. A transparent annual report wou

XX. Governance Model for a Semiconductor State

The semiconductor state is different from a conventional subsidy state. It does not merely provide fiscal incentives; it coordinates complex systems. Its role includes setting strategy, de-risking investment, building infrastructure, training talent, aggregating demand, enabling research, managing external partnerships and enforcing standards. This requires high administrative capacity. India should therefore upgrade the institutional capabilities of ISM and related agencies, ensuring that they are staffed with industry experts, technologists, financiers and project managers.

A strong governance model should distinguish between policy approval and industrial execution. Approval committees evaluate proposals, but execution teams solve daily bottlenecks. Semiconductor projects require rapid decisions on utilities, customs, visas, safety, environmental clearances, equipment logistics and supplier qualification. A single-window mechanism is useful only if it has real authority and technical competence. Otherwise it becomes another administrative layer.

State governments should be integrated through performance compacts. A state hosting a semiconductor project should commit to power quality, water systems, land readiness, local transport, housing, skilling, waste management and emergency response. In return, the central government can provide co-financing and technical support. This compact model would make state commitments measurable. It would also reduce the risk of states promising incentives without delivering operational readiness.

Policy stability is crucial because semiconductor investments have long horizons. Investors must trust that incentives, tax provisions, customs rules and procurement frameworks will not change unpredictably. India should provide long-term policy certainty while retaining performance accountability. A stable policy does not mean an inflexible policy; it means transparent rules, predictable review cycles and credible dispute resolution.

Data governance is also relevant. Semiconductor policy should be supported by accurate trade classification and demand data. If chip imports are poorly classified, policymakers cannot identify dependency risks. India should improve HS codes, customs data, strategic import tracking and demand forecasting. Better data would help identify which chips are critical, which sectors are most vulnerable and where localization makes economic sense.

Finally, governance should protect against hype. Semiconductor development attracts political attention, but excessive hype can distort strategy. The government should communicate progress honestly: construction is not production, production is not yield, yield is not profitability and profitability is not ecosystem depth. A mature semiconductor state distinguishes between milestones and outcomes. This honesty will build investor and public trust.

XXI. Scenario Analysis for 2030

Three scenarios can be imagined for India's semiconductor ecosystem in 2030. The first is the assembly-led scenario. In this scenario, India succeeds in attracting packaging and assembly facilities but remains heavily dependent on imported wafers, materials, substrates and designs. This scenario creates jobs and some strategic value, but domestic value addition remains limited. It is better than import dependence, but it does not fulfil the broader ambition of ecosystem capability.

The second is the balanced ecosystem scenario. India operates multiple packaging facilities, ramps at least one mature-node fab, supports domestic chip products, builds supplier depth in selected materials and creates a trained workforce. It remains globally interdependent but gains trusted capability in strategic domains. This is the most realistic and desirable 2030 scenario. It would make India a credible participant in global supply chains and reduce vulnerabilities in key sectors.

Table 6. Scenario matrix for India's semiconductor ecosystem in 2030

Scenario	Description	Implication
Assembly-led	Packaging scale grows but design, wafers and materials remain external.	Moderate jobs, limited value addition, partial resilience.
Balanced ecosystem	Packaging, mature-node fab, design products, supplier depth and talent pipelines mature together.	High strategic value, credible exports and lower critical dependence.
Fragmented subsidy	Multiple announcements but weak execution, low utilization and shallow local linkages.	High fiscal cost, limited capability and reduced investor confidence.

The third is the fragmented subsidy scenario. India announces many projects, but delays, talent gaps, weak supplier ecosystems and poor demand linkage prevent commercial success. Facilities remain isolated, capacity utilization is low and public incentives fail to create durable capability. This scenario is avoidable if policy shifts from announcement-driven ambition to milestone-based execution. It is the scenario against which governance must be designed.

The balanced ecosystem scenario requires disciplined choices. India should prioritize mature-node and specialized fabrication, ATMP/OSAT scale, compound semiconductors, design IP, reliability labs, supplier parks and talent pipelines. It should not dilute resources by chasing every segment simultaneously. Selectivity is not lack of ambition; it is the only way to convert ambition into capability.

XXII. Sectoral Applications: Where Indian Chips Should First Matter

A chip ecosystem becomes meaningful when it solves real sectoral problems. India should therefore define priority chip families around national applications rather than abstract technology categories. The most immediate applications are electric mobility, telecom infrastructure, energy systems, defence electronics, medical devices, industrial automation, secure digital infrastructure and consumer electronics. Each sector has different requirements for node, package, reliability, temperature range, certification and lifecycle. A demand-led strategy allows India to select technologies that have customers, rather than subsidizing capacity in search of demand.

In electric mobility, the priority is power electronics. EV powertrains require inverters, battery management systems, onboard chargers, DC-DC converters, thermal sensors and control units. Silicon carbide and gallium nitride devices can improve efficiency and reduce losses, while microcontrollers and analog chips manage safety and control. India should create a power electronics mission connecting EV manufacturers, battery firms, charger companies, power semiconductor startups and packaging units. This would support domestic value addition in a sector where India is already building scale.

Telecom and networking require a different strategy. India can focus on radio-frequency components, timing chips, network processors, optical communication devices, secure hardware modules and baseband-related design. Since telecom networks are critical infrastructure, trusted sourcing matters. India's domestic telecom equipment initiatives can become demand anchors for indigenous design and packaging. The policy objective should be a trusted telecom silicon stack, even if some advanced components remain globally sourced.

Table 7. Priority sectoral chip families for India by 2030

Sector	Priority chip families	Demand anchor
Electric mobility	SiC/GaN power devices, battery-management ICs, microcontrollers, sensors	EV manufacturers, charger networks, battery firms
Telecom and 6G	RF components, timing chips, network processors, optical and secure modules	Telecom equipment makers and public networks
Energy systems	Power management ICs, smart-meter chips, inverter control, grid sensors	Utilities, solar firms, storage and grid operators
Defence and space	Trusted microcontrollers, RF chips, secure elements, ruggedized sensors	Defence procurement, space missions and secure infrastructure
Medical devices	Analog front ends, sensors, low-power SoCs, secure data chips	Hospitals, med-tech firms and public health platforms
Consumer electronics	Display drivers, PMICs, connectivity chips, packaging services	Mobile, wearable and appliance manufacturers

Energy and grid modernization create demand for durable, high-reliability chips. Smart meters, solar inverters, storage systems, charging stations, industrial drives and grid-control devices require power management ICs, sensors, microcontrollers and communication chips. Public utilities can support market formation through procurement pilots and quality standards. The energy sector is particularly suitable for mature-node and power chips, making it a practical entry point for domestic design and packaging.

Defence and space demand must be handled with a security lens. These sectors often require ruggedization, long lifecycle support, secure supply, traceability and resistance to harsh environments. India should create specialized programs for trusted microcontrollers, secure elements, sensors, RF components and radiation-tolerant devices. The objective is not immediate full localization of every defence chip, but the creation of assured supply in categories where dependence creates operational vulnerability.

Medical devices and health technologies should not be overlooked. Diagnostic equipment, imaging systems, wearables, implantables, monitoring devices and point-of-care platforms require analog front ends, sensors, power management and secure data-processing chips. India has ambitions in affordable healthcare technology. Domestic semiconductor design for medical devices can reduce costs and improve supply assurance, provided reliability and certification standards are built early.

Consumer electronics remain the volume engine. Smartphones, wearables, appliances, tablets and smart-home devices generate high-volume demand for display drivers, power management chips, sensors, connectivity chips and packaging services. However, consumer electronics can also be price sensitive and globally competitive. India should use this sector for scale, while using strategic sectors for reliability and capability development. A balanced demand portfolio will reduce cyclicality.

Sectoral demand should be translated into chip roadmaps. For each priority sector, the government and industry should identify chip families, estimated demand, required technology nodes, package types, qualification standards, potential domestic designers, packaging partners and procurement channels. This would create a bridge between macro ambition and product-level execution. Without such product maps, the ecosystem may remain supply-push and fragmented.

XXIII. State Strategy and Cluster Specialisation

The role of Indian states will be decisive because semiconductor projects are physically embedded in state-level industrial systems. Land, power, water, local roads, policing, housing, labour support, training institutions and environmental implementation are all state functions or state-dependent. The central government can design incentives, but the investor experiences the state. Therefore, semiconductor federalism must be performance-oriented. States should compete not only on subsidy but on operational readiness.

Gujarat's early position comes from the clustering of Sanand and Dholera projects, strong industrial infrastructure and investor facilitation. The state can become a western semiconductor corridor if it builds supplier parks, advanced packaging labs, design offices, housing and training institutions around its anchors. The Dholera-Sanand axis should not be treated as two isolated locations; it should be planned as an integrated region with logistics, skills and supplier connectivity.

Assam's Morigaon project is strategically significant because it expands semiconductor manufacturing beyond established western and southern industrial corridors. Its success would demonstrate that high-technology manufacturing can support regional development in the North East. But this requires extraordinary attention to logistics, skilled workforce retention, supplier access, power quality and training. The state and central government should treat Morigaon as a model for inclusive semiconductor industrialization.

Uttar Pradesh has an opportunity through electronics manufacturing, the YEIDA/Jewar region, proximity to the National Capital Region and logistics infrastructure. If HCL-Foxconn/India Chip and related activities progress, the state can position itself in packaging, electronics components, design services and supplier ecosystems. However, it must build semiconductor-specific skills and utilities rather than relying only on general industrial attractiveness.

Odisha and other states can develop specialized niches such as advanced packaging, materials, chemicals, renewable-powered industrial parks and electronics components. Not every state needs a fab. Some states may become more successful by specializing in substrates, testing labs, design centres, equipment servicing, power electronics modules or chemical supply. A national cluster map should identify which state is best suited for which role.

Cluster specialization prevents wasteful duplication. If every state tries to announce a fab, resources will be spread thin and investor attention may be diluted. A stronger approach is a hub-and-spoke model: a few fab and packaging hubs supported by specialized supplier, talent and design nodes across the country. This would allow states to participate in the semiconductor economy without all chasing the same asset type.

State policy should include aftercare. Semiconductor investors need help after the memorandum of understanding is signed. Dedicated relationship teams should address construction, utilities, workforce, customs, safety, local community issues and supplier onboarding. In semiconductor manufacturing, aftercare may matter more than initial attraction. The states that solve operational problems fastest will build reputational advantage.

A Semiconductor Cluster Readiness Index should be published annually. It should score states on power reliability, water availability and recycling, land readiness, logistics, university linkages, skilling capacity, environmental systems, ease of permits, supplier ecosystem and industry aftercare. This index would move public debate from announcements to execution capability.

XXIV. Semiconductor Security and Trusted Supply Chains

Semiconductor security has two dimensions: availability and trust. Availability means that critical sectors can access required chips during global disruptions. Trust means that chips used in sensitive systems meet security, traceability and integrity requirements. India must build both. A purely commercial supply-chain strategy may reduce costs but leave strategic vulnerabilities. A purely autarkic strategy would be unrealistic and expensive. The practical path is trusted diversification combined with domestic capability in priority categories.

The government should classify chips by criticality. Tier one should include chips essential for defence, nuclear systems, telecom core networks, power grids, space, financial infrastructure and digital public infrastructure. Tier two should include chips important for automotive, health, railways, ports, aviation, energy and industrial systems. Tier three should include commercial consumer chips where global sourcing is acceptable. This classification would help determine where domestic production, trusted sourcing, inventory or certification is necessary.

Security also requires traceability. Chips used in critical systems should have documented supply chains, trusted packaging, secure firmware, anti-tamper features where needed and validation against counterfeit risks. India should strengthen testing labs for counterfeit detection, hardware security evaluation and supply-chain assurance. These labs can support both government procurement and private industry.

Export controls and geopolitical fragmentation must be treated as permanent variables. Access to advanced tools, EDA software, materials or IP may be affected by external policy decisions. India should therefore diversify partnerships and avoid dependency on any single country or supplier. Trusted partnerships with multiple jurisdictions can create resilience. The goal is to be aligned with global rules while preserving national flexibility.

A national semiconductor reserve may be necessary for selected categories. This does not mean stockpiling every chip, which would be costly and technologically inefficient. It means identifying critical long-lifecycle chips for infrastructure and defence, then maintaining inventory or assured production arrangements. The reserve should be dynamic and linked to obsolescence planning.

Hardware security should be integrated with India's cyber policy. Secure software cannot fully compensate for compromised hardware. As AI, telecom and public infrastructure expand, trusted hardware becomes a prerequisite for secure digital systems. Semiconductor policy should therefore be coordinated with cybersecurity, defence procurement and critical infrastructure regulation.

India's trusted supply-chain proposition can become an export advantage. Global firms are looking for reliable locations outside excessive concentration. If India demonstrates rule of law, security standards, quality systems and geopolitical trust, it can attract customers seeking resilient supply chains. Trust is not just a diplomatic label; it is an industrial capability built through standards, audits and performance.

XXV. Export Strategy and Global Value Chain Integration

India's domestic market is large, but semiconductor projects need global integration to reach scale. Packaging units and fabs require high utilization. Domestic demand alone may not be sufficient in the early years, especially for specialized facilities. Therefore, export strategy should be built into project planning from the beginning. Facilities should identify global customer segments, certification needs, logistics channels and pricing benchmarks before production starts.

Export credibility depends on quality and delivery. Semiconductor customers audit suppliers intensely. They examine process control, reliability, traceability, environmental standards, labour practices, cybersecurity, business continuity and financial stability. India should help facilities prepare for global audits through national quality programs and expert support. Export promotion in semiconductors is not about trade fairs alone; it is about passing customer qualification.

India can position itself as a trusted back-end and specialized manufacturing location. ATMP, OSAT, discrete devices, power electronics, sensors and mature-node chips can serve global customers seeking supply-chain diversification. The country can also offer design-to-package services, combining Indian design talent with domestic packaging. This integrated offering could differentiate India from locations that provide only one layer.

Trade policy should support semiconductor integration. Customs systems must handle sensitive equipment and inputs quickly. Tariff policy should avoid raising costs for inputs that are not domestically available. At the same time, incentives can encourage localization where domestic suppliers meet quality standards. The objective should be competitiveness, not protectionism for its own sake.

Standards diplomacy matters. India should participate actively in international semiconductor standards, reliability forums, electronics safety systems and trusted technology partnerships. Standards participation gives Indian firms early knowledge of market expectations and helps domestic products gain acceptance. It also supports India's image as a serious semiconductor jurisdiction.

Brand India in semiconductors should be built around reliability, trust, engineering talent and democratic supply-chain diversification. India should avoid overpromising leading-edge dominance. A more credible message is that India will become a dependable partner for mature-node chips, advanced packaging, compound semiconductors, design services, embedded products and trusted electronics. Credible positioning will attract better partners than exaggerated claims.

Export strategy should also include regional markets. South Asia, Africa, the Middle East and Southeast Asia will expand electronics, telecom, energy and mobility infrastructure. Indian-designed and packaged chips embedded in affordable devices can serve these markets. This aligns semiconductor policy with India's broader development partnerships and South-South cooperation.

XXVI. Monitoring, Evaluation and Success Metrics

A national mission should define success metrics clearly. The easiest metrics are investment value and number of projects approved, but these are input indicators. India must track output, capability and resilience indicators. A semiconductor mission that spends money but does not create operational capability would fail the strategic test. Evaluation should therefore measure production, yield improvement, customer qualification, exports, domestic value addition, supplier localization, talent and strategic availability.

The first metric is operational status. Projects should be classified as announced, under construction, tools installed, pilot production, qualified production, commercial production and export-qualified production. This avoids confusion between early-stage announcements and actual output. It also helps identify bottlenecks at each stage. Public reporting can be aggregated to protect commercial sensitivity while still providing accountability.

The second metric is domestic value addition. A packaging facility that imports wafers, substrates, chemicals and equipment but performs assembly in India has a different value profile from a facility that sources packaging materials, testing services and design support domestically. Value-add measurement should be gradual and realistic. The aim is not to punish early-stage import dependence but to ensure that localization deepens over time.

The third metric is talent. India should report the number of trained process engineers, equipment technicians, packaging specialists, design engineers, reliability engineers and cleanroom operators. It should also track placement, retention and cluster distribution. Talent metrics will reveal whether education programs are aligned with industry needs.

Table 8. Mission metrics for annual semiconductor ecosystem review

Metric	What to measure	Recommended instrument
Project execution	Stage from announcement to export-qualified production	Quarterly milestone review
Domestic value addition	Local content in packaging, materials, testing, design and services	Annual supplier and value-add audit
Talent pipeline	Number of certified technicians, engineers and specialists	Cluster-wise training dashboard

Metric	What to measure	Recommended instrument
Design commercialization	DLI designs deployed in products and revenue generated	Prototype-to-product tracking
Strategic resilience	Trusted supply status for critical chip categories	National semiconductor security scorecard
Environmental performance	Water recycling, waste handling, energy quality and community safeguards	Independent environmental audit

The fourth metric is design deployment. The number of tape-outs is useful, but deployed chips matter more. India should track DLI-supported designs that reach prototypes, customer trials, qualification, commercial deployment and revenue. It should also track IP reuse and exports. This would shift incentives from symbolic innovation to market innovation.

The fifth metric is resilience. Strategic sectors should report whether critical chip categories have trusted supply, domestic alternatives, inventories or qualification pathways. A resilience scorecard would help national security planners and industrial policymakers work together. It would also identify where urgent capability building is needed.

The sixth metric is environmental performance. Water recycling, energy mix, chemical safety, waste treatment and community engagement should be tracked. Semiconductor manufacturing can be sustainable if planned well. Environmental metrics will strengthen social legitimacy and export credibility.

Evaluation should be independent and technical. India can create an annual review panel including industry experts, academics, financial analysts and former project managers. The panel should assess progress and recommend course corrections. Public missions succeed when they learn; they fail when they defend old assumptions.

XXVII. Research Agenda for Universities, Think Tanks and Industry

India's semiconductor mission should be supported by a research agenda that is practical, interdisciplinary and linked to industrial deployment. Universities and think tanks should not treat semiconductors only as an engineering topic. The ecosystem also raises questions of industrial policy, trade, federalism, environmental governance, workforce development, national security, finance, standards and international cooperation. A serious 2030 strategy requires evidence from all these domains.

The first research priority is demand mapping. India needs product-level studies of chip requirements in EVs, telecom, defence, energy, medical devices, railways, drones, smart agriculture and digital public infrastructure. These studies should identify volumes, technology nodes, package types, import sources, qualification standards and potential domestic alternatives. Without such granular demand research, policy will depend on aggregate market estimates that are too broad for investment decisions.

The second priority is supplier capability mapping. Research institutions should identify Indian firms that can enter semiconductor-adjacent supply chains: chemicals, gases, substrates, cleanroom services, precision engineering, high-density PCBs, testing equipment, thermal materials, packaging inputs, logistics and maintenance. Each supplier category should be evaluated for quality gaps, capital needs, certification requirements and partnership opportunities. Supplier research can convert vague localization goals into actionable industrial programs.

The third priority is talent analytics. India needs better data on how many engineers and technicians are required by node, process, package type and cluster. Universities should study curriculum gaps and benchmark Indian training programs against Taiwan, Singapore, South Korea and the United States. Talent policy should be evidence-based, because overproduction of generic graduates and underproduction of fab-ready technicians would both harm the mission.

The fourth priority is environmental and resource research. Semiconductor projects require water, energy, chemical handling and waste systems. Indian researchers should develop models for water recycling, green power procurement, chemical safety and community impact. This research must be region-specific because water stress, grid quality and environmental sensitivity differ across clusters. Sustainable semiconductor manufacturing should be a research objective, not a compliance afterthought.

The fifth priority is semiconductor security. Think tanks should assess critical chip dependencies in defence, telecom, energy, finance, transport and public digital systems. They should develop frameworks for trusted sourcing, hardware assurance, counterfeit detection, inventory policy and supply-chain resilience. Semiconductor security requires technical knowledge and strategic analysis. It should not be left to either engineers or security analysts alone.

Table 9. Research agenda to support India's semiconductor mission

Research area	Core question	Policy use
Demand mapping	Product-level chip demand across EV, telecom, defence, energy, health and infrastructure	Investment prioritization and procurement planning
Supplier capability	Domestic firms in materials, gases, substrates, cleanroom services and equipment support	Localization roadmaps and supplier development
Talent analytics	Fab-ready roles, curriculum gaps and cluster-wise workforce needs	Targeted skilling and university reform
Environmental systems	Water recycling, energy reliability, chemical safety and community safeguards	Sustainable cluster planning
Security analysis	Critical chip dependencies and trusted supply requirements	National semiconductor security framework
Finance research	Project finance, risk guarantees and public return on investment	Better capital allocation and risk sharing

The sixth priority is comparative industrial strategy. India should systematically study how Taiwan built foundry strength, how Japan built materials leadership, how South Korea developed memory scale, how the United States retained design and EDA dominance, and how the European Union links chips to automotive and industrial demand. Comparative research should avoid superficial imitation and identify transferable institutional mechanisms.

The seventh priority is finance and risk. Semiconductor investments need patient capital, foreign exchange planning, insurance, risk guarantees and milestone-linked public support. Indian financial researchers should develop models for semiconductor project finance, including revenue risk, technology risk, utilization risk and public return on investment. Better finance research would help banks, development finance institutions and investors evaluate projects more intelligently.

The eighth priority is standards and quality. Indian institutions should study reliability standards for automotive, industrial, medical, telecom and defence chips. They should help create testing protocols, certification pathways and quality benchmarks. Standards research is essential because market acceptance depends on trust. A chip that cannot pass customer qualification cannot become an ecosystem asset.

Finally, the research agenda should be institutionalized. India should create a Semiconductor Policy and Technology Observatory that publishes annual reports, datasets, case studies and policy briefs. It should work with ISM, industry, states and universities while maintaining analytical independence. Such an observatory would help the mission learn continuously, avoid policy blind spots and translate global developments into Indian strategy.

XXVIII. Discussion

India's semiconductor ambition is credible because it rests on real demand, policy commitment, engineering talent and geopolitical opportunity. It is not yet secure because ecosystem depth takes time. The difference between credibility and success will be determined by execution. The early signs are encouraging: a large incentive framework, major approved projects, design support, electronics manufacturing growth and the launch of ISM 2.0. But the next phase will be harder. It involves the unglamorous work of utilities, training, supplier qualification, yield learning, reliability testing and customer acquisition.

A key insight is that India should not frame the semiconductor race as a single ladder with leading-edge logic at the top. The industry is diversifying. AI increases demand for advanced chips, but EVs, telecom, industrial automation, energy systems and defence require a wide range of mature, analog, power, sensor and packaging capabilities. India's 2030 opportunity lies in this diversified landscape. It can become globally relevant by being reliable, specialized and integrated with demand.

The paper also suggests that semiconductor policy should be linked to India's wider development strategy. Chips should support domestic electronics value addition, energy transition, mobility, defence, digital governance, health technologies and industrial modernization. If semiconductor facilities are integrated into these sectors, the ecosystem will have domestic anchors. If not, it will depend excessively on export markets and global cycles. Domestic demand is India's strategic advantage; it must be organized into bankable industrial demand.

Another insight concerns institutional capacity. Semiconductor development requires a developmental state with technical competence. India has experience with digital public infrastructure and large-scale public missions, but semiconductor manufacturing requires different capabilities. It demands industrial project management, technology assessment, supply-chain finance, export market knowledge and environmental specialization. Building state capacity is therefore part of building the chip ecosystem.

The most important strategic choice is to build from strengths while addressing gaps. India's strengths are software, design talent, domestic demand, electronics assembly, democratic trust and partnership potential. Its gaps are fabrication experience, supplier depth, equipment services, materials, process talent and patient capital. A successful strategy will connect strengths to gaps: use domestic demand to attract fabs, use design talent to create products, use partnerships to gain process know-how, use electronics scale to deepen components, and use public policy to coordinate the system.

By 2030, India should be judged by whether global firms see it as a reliable semiconductor location, whether domestic firms can design and deploy chips, whether strategic sectors can access trusted supply, and whether clusters have developed specialized supplier ecosystems. If these outcomes are achieved, India will have moved from semiconductor ambition to semiconductor capability.

XXIX. Conclusion

India's semiconductor ambition is one of the most consequential industrial projects of the decade. It is driven by a convergence of domestic demand, technological change, geopolitical realignment and national development priorities. Chips are no longer simply inputs into electronics; they are the infrastructure of artificial intelligence, telecom, defence, energy, mobility, health and digital governance. For India, building a chip ecosystem by 2030 is therefore both an economic opportunity and a strategic necessity.

The paper has argued that India's best pathway is ecosystem-led and differentiated. India should not define success solely by the most advanced logic node. It should build strength in mature-node fabrication, ATMP and OSAT, advanced packaging, compound semiconductors, power electronics, sensors, design IP, materials, equipment services, reliability infrastructure and talent. This approach aligns with India's demand profile and current project pipeline. It also positions India for the More-than-Moore era, where system integration and packaging matter as much as transistor scaling.

The policy architecture is now substantial. The India Semiconductor Mission, fiscal support schemes, Design Linked Incentive, electronics manufacturing policies and ISM 2.0 provide a foundation. Major projects in Gujarat, Assam and other emerging clusters show that investment has begun. But the decisive test lies ahead. Construction must become production; production must become yield; yield must become customer trust; customer trust must become ecosystem depth. Each transition requires governance discipline.

The recommendations in this paper emphasize mission governance, demand aggregation, supplier parks, fab-ready skilling, design commercialization, reliability labs, environmental trust and global partnerships. These are not peripheral measures; they are the core of semiconductor success. A fab without suppliers, talent and customers is incomplete. A design without packaging and deployment is incomplete. A policy without execution is incomplete. India's task is to complete the system.

If India follows a sequenced and disciplined roadmap, it can become a trusted semiconductor ecosystem by 2030. It may not control every layer of the global value chain, but it can become indispensable in selected layers. It can reduce critical dependence, raise domestic value addition, create high-skill jobs, support strategic sectors and participate in global supply chains with confidence. The ambition is difficult, but it is no longer speculative. The next five years will determine whether India becomes merely a large chip market or a genuine chip ecosystem.

XXX. Acknowledgment

The author acknowledges the public availability of official policy documents, press releases and industry analyses that make transparent policy research possible. The views expressed in this paper are analytical and do not represent any official position of any government agency or private entity.

References

[1] India Semiconductor Mission, “Schemes: Semiconductor fabs, display fabs, compound semiconductor and ATMP, and design linked incentive,” official website, accessed June 2026.

[2] Press Information Bureau, Government of India, “India Semiconductor Mission 2.0: A major push in Budget 2026 towards semiconductor self-reliance,” February 7, 2026.

[3] Press Information Bureau, Ministry of Electronics and IT, “Budget 2026-27 announces the launch of India Semiconductor Mission 2.0,” February 1, 2026.

[4] Press Information Bureau, Cabinet, “Giant leap for India Semiconductor Mission: Cabinet approves three more semiconductor units,” February 29, 2024.

[5] Press Information Bureau, Cabinet, “Cabinet approves one more semiconductor unit under India Semiconductor Mission,” September 2, 2024.

[6] Prime Minister’s Office, Government of India, “Cabinet approves two more semiconductor manufacturing units with cumulative investment of more than Rs.3,900 crore,” May 5, 2026.

[7] Press Information Bureau, “India’s Semiconductor Revolution: Powering the future of electronics,” August 3, 2025.

[8] Press Information Bureau, “Design Linked Incentive Scheme,” January 4, 2026.

[9] Design Linked Incentive Scheme, “EDA Tool Grid and ChipIN infrastructure,” official portal, accessed June 2026.

[10] Press Information Bureau, Ministry of Electronics and IT, “India emerges as second largest mobile manufacturing country; smartphone exports lead in 2025,” March 11, 2026.

[11] Deloitte, “2026 semiconductor industry outlook,” Deloitte Insights, February 2026.

[12] McKinsey & Company, “Hiding in plain sight: The underestimated size of the semiconductor industry,” January 15, 2026.

[13] Deloitte India, “Beyond AI hype, India scales compute and semiconductors,” TMT Predictions 2026 press release, 2026.

[14] NITI Aayog, “Future of India’s Semiconductor Industry,” NITI Frontier Tech Hub, May 2026.

[15] NITI Aayog, “Electronics: Powering India’s participation in global value chains,” July 2024.

[16] World Semiconductor Trade Statistics, “Global semiconductor market approaches USD 1 trillion in 2026,” WSTS Autumn Forecast, 2025.

[17] Semiconductor Industry Association, “Global semiconductor sales and WSTS forecast commentary,” market data release, 2025.

[18] Ministry of Electronics and IT, “Production Linked Incentive Scheme for large scale electronics manufacturing,” official scheme material, Government of India.

[19] Government of India, “Scheme for Promotion of Manufacturing of Electronic Components and Semiconductors,” policy material, MeitY.
[20] Information Technology and Innovation Foundation, “Assessing India’s semiconductor readiness,” 2024.
[21] Deloitte and industry analyses, “India semiconductor market and investment outlook,” 2025-26.
[22] India Electronics and Semiconductor Association, “India semiconductor market and ecosystem reports,” research portal, accessed June 2026.
[23] Organisation for Economic Co-operation and Development, “Semiconductor supply chains, industrial policy and strategic dependencies,” policy analysis, various years.
[24] World Bank, “Global value chains and manufacturing competitiveness,” policy research material, various years.
[25] Asian Development Bank, “Industrial corridors, skills and technology-led manufacturing in Asia,” policy research material, various years.

Annexure: Implementation Checklist for 2026 to 2030

A practical 2030 strategy should convert each recommendation into an institutional checklist. The first checklist concerns project readiness. Each approved facility should be tracked against land transfer, boundary completion, cleanroom contractor appointment, power redundancy, water recycling design, effluent treatment, equipment import approvals, technology partner staffing, local hiring, safety protocols and customer engagement. These readiness indicators should be updated quarterly within the mission structure.

The second checklist concerns supplier development. Anchor facilities should identify their top one hundred recurring inputs by value and criticality. These should be divided into inputs that can be localized within two years, inputs that require joint ventures, and inputs that must be secured through long-term import agreements. For each input, India should identify potential domestic suppliers, quality gaps, certification requirements and investment needs. Supplier development must be treated as a program, not as a voluntary spillover.

The third checklist concerns talent. Every semiconductor cluster should map required job roles for the next five years. Training capacity should be created before hiring pressure peaks. A model curriculum should cover cleanroom discipline, tool operation, ESD safety, process control, reliability, documentation, English technical communication and emergency procedures. Apprenticeships should be embedded in project contracts. Worker housing and transport should also be planned because semiconductor facilities operate around the clock.

The fourth checklist concerns design commercialization. DLI-supported firms should be mapped to product sectors such as EVs, telecom, energy, defence, medical devices and consumer electronics. Each firm should have access to a packaging partner, testing lab, reference customers and commercialization finance. Public agencies can support pilot procurement where security or public-service needs justify domestic development. The goal is to prevent promising designs from remaining trapped between prototype and market.

The fifth checklist concerns environmental assurance. Water sourcing, recycling, chemical storage, hazardous waste handling, emissions monitoring and emergency response should be standardized across clusters.

Environmental compliance should be digital, transparent and technically competent. Communities should receive clear information on water use, jobs, safety and local benefits. Sustainable industrialization will be essential for the legitimacy of semiconductor clusters.

The sixth checklist concerns global integration. India should identify target countries and firms for each ecosystem gap: Taiwan for foundry know-how and supplier discipline, Japan for materials and equipment ecosystems, the United States for design and EDA, South Korea for memory and manufacturing scale, Europe for automotive and industrial semiconductors, and Singapore for operations and logistics. Partnerships should be tied to measurable capability outcomes.

The seventh checklist concerns security. India should identify strategic chips used in defence, telecom, energy, digital public infrastructure, financial systems and transport. For each chip category, it should define the acceptable level of domestic capability, trusted sourcing, inventory and substitution. Semiconductor security should be integrated into national security planning, cyber resilience and critical infrastructure protection.

The eighth checklist concerns measurement. An annual dashboard should report projects under execution, commercial output, domestic value addition, export performance, supplier localization, trained personnel, number of deployed domestic designs, water recycling performance, patents, reliability certifications and strategic chip availability. Transparent measurement would improve accountability and prevent narrative-driven policy evaluation.